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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,677	04/21/2004	Matthew A. Ahrens	03226.393001; P8512	4465

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,677	AHRENS ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/828,677 has a total of 22 claims pending in the application; there are 4 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-11, 13-15 and 17-22** are rejected under 35 U.S.C. 102(b) as being anticipated by Talangala et al. (US 2002/0161972).

6. As per **claims 1, 13 and 21-22**, Talangala discloses

"A method/system/network system having a plurality of nodes for dynamic striping, comprising:" as **["dynamic striping may be employed so that new writes form new parity group. Thus, stripes of various sizes may be supported by the storage system" (Column 2, paragraph 0012)]**

"a processor" [With respect to this limitation, Talangala discloses "main processor 100" (Figure 2)]

"a memory" [Talangala discloses this limitation as "system memory 200" (Figure 2)]

"a storage device" [This limitation is disclosed by Talangala as "data storage subsystem 400" (Figure 2)]

"software instructions stored in the memory for enabling the under control of the processor, to:" **[With respect to this limitation, Talangala discloses "To facilitate keeping track of the data and parity information, a block remapping technique may be implemented in software and/or hardware which maps a logical or virtual block address to a physical storage device segment" (Column 6, paragraph 0054 and Column 3, paragraph 0033, lines 21-26)]**

"receiving a request to write a data block into a storage pool;" **[With respect to this limitation, Talangala discloses "receiving a write transaction specifying the virtual addresses of a subset of the data blocks of a data stripe" (Column 3, paragraph 0017 and Column 6, paragraph 0059)]**

"determining a physical disk location in the storage pool to store the data block using a dynamic striping policy;" **[With respect to this limitation, Talangala discloses that "With dynamic striping, the host machine, the host machine interacts with the storage array via virtual**

addresses" and explains that "When a block is written, a physical location is chosen for it" (Column 6, paragraph 0059). Talangala also discloses having a "free segment bitmap" used to "keep track of all physical segments on all storage devices" to allocate new data to free/empty segments (Column 5, paragraph 0051)]

"storing the data block at the physical disk location; and storing a first indirect block in the storage pool, wherein the first indirect block comprises the data block location and the data block checksum" **[Talangala discloses this limitation as "An indirection map (e.g. block remapping table) matches virtual block addresses to physical block addresses. Block-level checksums may be provided in the indirection map" (Column 6, paragraph 0059 and Figure 6C)]**.

7. As per **claim 2**, Talangala discloses "The method of claim 1," **[See rejection to claim 1 above]** "further comprising: retrieving the data block using the first indirect block" **[With respect to this limitation, Talangala disclose that "when a block read is requested, the block's indirection map entry is read to find the block's physical address" (Column 7, paragraph 0061, lines 8-10)]**.

8. As per **claim 3**, Talangala discloses "The method of claim 1," **[See rejection to claim 1 above]** "further comprising: assembling the first indirect block, wherein assembling the first indirect block comprises populating a block pointer" **[Talangala discloses this concept as "a hash indirection table (HIT)" which "maps virtual block addresses to an entry or index number in a parity group table" (Column 6, paragraphs 0054-0055 and Figures 6B, 7A, 8A, 6C, 7B and 8B). Note that each virtual address in "HIT" maps to an entry in "PGT**

(parity group table)" and that each field in PGT table stores configuration information for each "indirect block"].

9. As per **claim 4**, Talangala discloses "The method of claim 3," **[See rejection to claim 3 above]** "wherein populating the block pointer comprises: storing the data block checksum in a checksum field within the block pointer;" **[Talangala discloses this concept as "each block's checksum is stored in an entry in the indirection map, e.g. as part of a block remapping table entry (e.g. PGT entry) for each block" (Column 6, paragraph 0058, lines 4-6 and Figures 6C, 7B and 8B) wherein each entry representing/pointing to a block in PGT contains a checksum in a checksum field]**

"and storing the data block location in the block pointer, wherein storing the data block location comprises storing a metaslab ID" **[Talangala discloses this concept as "HIT (Hash Indirection Table)" which contains "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups/stripes/metaslabs such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B). Talangala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein "this may be interpreted as Disk 1, segment 132" (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)]** "and offset" **[Talangala discloses this concept as entries stored under the "Next Entry In Parity Group" field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)]**.

10. As per **claim 5**, Talangala discloses "The method of claim 4," **[See rejection to claim 4 above]** "further comprising: storing a birth value in a birth field within the block pointer". **[Talangala discloses this concept as an embodiment having a "HIT (hash indirection table) which maintains generational images" and explains that "the PGT index columns are now labeled version zero through version two, where version zero corresponds to the most current version and version two corresponds to the oldest version" (Column 7, paragraph 0065 and Figures 8A and 8B)]**.

11. As per **claims 6 and 15**, Talangala discloses "The method/system of claims 3 and 13," **[See rejection to claim 3 and 13 above]** "wherein the first indirect block is assembled using a data management unit" **[With respect to this limitation, Talangala discloses "Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033)]**.

12. As per **claims 7 and 17**, Talangala discloses "The method/system of claims 1 and 13," **[See rejection to claims 1 and 13 above]** "wherein the storage pool comprises at least one storage device" **[With respect to this limitation, Talangala discloses "Array of Storage Devices 410" (Figures 2 and 3)]**.

13. As per **claims 8 and 18**, Talangala discloses "The method/sytem of claims 1 and 13," **[See rejection to claims 1 and 13 above]** "wherein the storage pool is divided into a plurality of metaslabs" **[With respect to this limitation, Talangala discloses having different "stripes of data" within an array storage devices (Figure 4 and Column 4, paragraph 0043) and explains that a "stripe" of data is analogous to a "parity group" (Column 7, paragraph 0063, lines 10-11) wherein configuration information for each of the "parity groups" is**

stored in a "PGT (parity group table)" (Figures 6C, 7B and 8B) which are equivalent to "metaslabs" as claimed by Applicant].

14. As per **claims 9 and 19**, Talangala discloses "The method/system of claims 8 and 18," **[See rejection to claims 8 and 18 above]** "wherein each of the plurality of metaslabs is associated with a metaslab ID" **[Talangala discloses this concept as each virtual block has a virtual address which is used to access a "HIT (Hash Indirection Table)" which contains "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups/stripes/metaslabs such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].**

15. As per **claims 10 and 20**, Talangala discloses "The method of claims 9 and 19," **[See rejection to claims 9 and 19 above]** "wherein the data block location comprises the metaslab ID and an offset" **[Talangala discloses this concept as each virtual block has a virtual address which is used to access a "HIT (Hash Indirection Table)" which contains "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups/stripes/metaslabs. Talangala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein "this may be interpreted as Disk 1, segment 132" (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].** Talangala also discloses **["Next Entry In Parity Group" field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B) as an offset].**

16. As per **claim 11**, Talangala discloses "The method of claim 1," **[See rejection to claim 1 above]** "wherein storing the data block comprises using a storage pool allocator" **[With respect to this limitation, Talangala discloses "Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033)]**.

17. As per **claim 14**, Talangala discloses "The system of claim 13," **[See rejection to claim 13 above]** "further comprising: a second indirect block, comprising a first indirect block checksum and a first indirect block location, wherein the storage pool allocator is further configured to store the second indirect block in the storage pool" **[With respect to this limitation, Talangala discloses writing a block having a checksum and a location in PGT (Parity Group Table) which have a "segment" field to store a location and a "checksum" field to store a checksum (Column 6, paragraph 0059 and Figures 6C, 7B and 8B) and provides (Figures 6C, 7B and 8B) which contain parity/stripe group tables having entries for multiple blocks of data stored in a storage pool]**.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. **Claims 12 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Talangala et al. (US 2002/0161972) in view of Dalal et al. (US 2004/0123063).

As per **claims 12 and 16**, Talangala discloses "The method/system of claims 1 and 13," **[See rejection to claims 1 and 13 above]** wherein the dynamic striping policy comprises a dynamic striping policy based on free space available on physical disks as **["With dynamic striping, the host machine, the host machine interacts with the storage array via virtual addresses" (Column 6, paragraph 0059) and teaches having a "free segment bitmap" used to "keep track of all physical segments on all storage devices" to allocate new data to free/empty segments (Column 5, paragraph 0051) as using a dynamic striping policy based on free space available on disks]**. However, Talangala fails to disclose expressly that "the dynamic striping policy comprises at least one selected from the group consisting of a dynamic striping policy based on physical disk speed, a dynamic striping policy based on free space available on physical disks, a dynamic striping policy based on load on physical disks, and a round robin policy."

Dalal discloses "the dynamic striping policy comprises at least one selected from the group consisting of" different "dynamic striping" policies such as policies "based on physical disk speed, a dynamic striping policy based on free space available on physical disks, a dynamic striping policy based on load on physical disks, and a round robin policy" as **["Allocation coordinator 1010 obtains data form configuration database 1004, which includes data about templates, capabilities, rules and policy database 1006, which contains information about storage environment policies. An example of a policy is a specification of a stripe unit width for creating columns in a striped virtual object" and explains that "allocation coordinator 1010 also obtains information about the available storage environment from storage information collector" (Column 6, paragraph 0102 and Column 12, paragraph**

0187) as having rules to allocate storage based on available storage space. Dalal also teaches that "striped storage has capacity, maximum bandwidth, and maximum I/O rate that is the sum of the corresponding values of its constituent disks" (Columns 13-14, paragraph 0213) wherein "optimum stripe unit size must be determined on a case-by-case basis, taking into account access patterns presented by the applications that will use striped storage" (Column 14, paragraph 0215) as taking into account, storage capacity, bandwidth and I/O rate to stripe storage devices].

Talangala et al. (US 2002/0161972) and Dalal et al. (US 2004/0123063) are analogous art because they are from the same field of endeavor of striping storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the dynamic striping system as taught by Talangala and further stripe storage devices by selecting rules as taught by Dalal.

The motivation for doing so would have been Dalal teaches that using certain rules to stripe a storage device **["enable the device to provide certain capabilities, such as high performance, inherently" and explains that "to ensure that logical volume meets user requirements, a combination of physical characteristics of some storage devices and software configuration of other storage devices using rules can be used to provide all capabilities meeting the user requirements" (Column 6, paragraph 0100)]**.

Therefore, it would have been obvious to combine Dalal et al. (US 2004/0123063) with Talangala et al. (US 2002/0161972) for the benefit of creating a system/method for dynamic striping to obtain the invention as specified in claims 12 and 16.

IV. RELEVANT ART CITED BY THE EXAMINER

20. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

21. The following reference teaches using striping rules when expanding storage capacity.

U.S. PATENT NUMBER

US 2003/0145167

22. The following reference teaches file-level striping.

U.S. PATENT NUMBER

US 2004/0107314

23. The following reference teaches dynamic striping.

U.S. PATENT NUMBER

US 6,745,284

US 2005/0097270

US 2003/0033477

24. The following reference teaches striping in a network environment.

U.S. PATENT NUMBER

US 2002/0004883

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

25. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

26. Per the instant office action, **claims 1-22** have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

28. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 21, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER